EMBEDDED COMPUTING CONFERENCE

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Presentation

Title:	Dataflow Programming on Configurable Many-Core Architecture: a Result of Software-Hardware Codesign
Target Audience:	Developers
Presenters/ Universities:	Lisa (Ling) Liu, Computer Systems Institute, ETH, Zürich Oleksii Morozov, Physics in Medicine Research Group, University Hospital of Basel
Abstract:	This presentation presents the design and implementation of a hybrid dataflow programming environment and a configurable many-core architecture. The principal difference between our approach and other dataflow programming environments is that the compiler generates not only instruction sequences, but also the target machine's architecture, a many-core processor with configurable interconnect circuits, I/O interfaces and on-chip local memories of each core. The many-core processor is then implemented on Xilinx Virtex-5XC5VLX50T FPGA via Xilinx ISE tools. The advantage of this approach is that the target machine is tailored for the application to achieve better performance and power efficiency. To prove the applicability of our approach, a monitor for real-time ECG signal analysis was built and analyzed for ist performance, size and power consumption.