Automation der Zukunft dank 1 GBit Industrial Ethernet.
Gigabit Ethernet
in
High-Speed
Embedded Systems
INDustrielle ELektronik
Customized automation
- since 1974
Product Lifecycle
Infotech IP-500

30% growth per year

Factor 8 in 9 years

4 axes → 32 axes

2003 → 2012
Choose a fieldbus with buffer. Choose Gigabit.
ESEC Die Bonder (semiconductors): Speed & Precision.

Source: www.avista.ch
1 Master

10 Slaves
37 axes, 450 IOs (analog, digital, heating unit, ...)

1 GBit/s Ethernet (copper)

GinLink: Indel high-speed, real-time fieldbus.

Master / Slave architecture.
Ring topology. Other topologies possible.
Data flow: From **master through slaves** back to the master.
High-Speed fieldbus means: low cycle time. But how to calculate it?
37 axes, 450 IOs: **3000 Bits** per Ethernet frame

Cycle time: depends on **data bandwidth** (1 GBit/s).
Cycle time
Bandwidth only

1 Bit  1 ns
3000 Bit  3.0 µs
20m cable  0.1 µs
Data travels through slaves. Each Slave causes latency.
**Cycle time**
Including slave latency

<table>
<thead>
<tr>
<th>3000 Bit</th>
<th>10 Slaves</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0µs</td>
<td>4.5µs</td>
</tr>
<tr>
<td>7.5µs</td>
<td></td>
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60%
On-the-fly data reading

Receive value from master

Send actual value to master

On-the-fly data exchange
Application layer in FPGA guarantees **maximum performance**.
The PHY makes the difference.
(Gigabit) **PHY facts**

**Power** consumption about 1/3 compared to 2008

**Latency** rarely in **datasheet**

**Not** optimized for latency
How does the **Master** influence the cycle time?
Ethernet frame creation and transmission by FPGA not CPU.
Store newest slave data in receive buffer
Assert IRQ at CPU

Real-time task(s)

INT
Read newest slave values from FPGA

Real-time task(s)
Calculate new slave values: PID, logic, algorithms
Write new slave values to FPGA transmit buffer
Put new slave values into Ethernet frame
Master facts

Data RX/TX **decoupled** from **CPU/software**

Timing 100% **deterministic**

Save CPU **performance**

Put new slave values into Ethernet frame
The Application defines the master processing time.
RTOS facts

Custom real-time OS tailored to Indel hardware

Optimized for automation

Optimized for maximum performance
Cycle time mainly defined by Master CPU load (assuming few slaves).
Cycle time diagram

11 Devices
3000 Bit
Application

FPGA & PHY latency
Data transmission time
PID / Logic / Algorithms

5 µs
3 µs
46 µs + 8.5 µs
62.5 µs (16 kHz)
What’s the benefit of Gigabit Ethernet?
What’s the benefit of Gigabit Ethernet?

Showdown: **3000 Bit @ 62.5 µs**

- **11 Devices**
  - **3000 Bit**
  - **Application**

- **5 µs**
- **55 µs**

**3000 Bit @ 30 µs**

- **1 G vs. 100 M**
- **5 µs**
- **30 µs**

Transferring 3000 Bit takes **10 times less** thanks to Gigabit Ethernet.
What’s the benefit of Gigabit Ethernet?

Showdown: 3000 Bit @ 62.5 µs

11 Devices
3000 Bit
Application

5 µs
11 Devices
3000 Bit
Application

55 µs

1 G vs. 100 M

28 µs

The application has much more time thanks to Gigabit Ethernet.
What's the benefit of Gigabit Ethernet?

Showdown: **20 Slaves, 6000 Bit @ 62.5 µs**

The more data the bigger the benefit of Gigabit Ethernet.
What's the benefit of Gigabit Ethernet?

Showdown: 20 Slaves, 6000 Bit @ 62.5 µs

21 Devices | 6000 Bit
---|---
Application | 9 µs

1 G vs. 100 M

9 µs | 60 µs

-6 µs

There's no more time for the application with 100 MBit Ethernet.
What's the benefit of Gigabit Ethernet?

The faster the cycle time, the bigger the benefit of Gigabit Ethernet.
What’s the benefit of Gigabit Ethernet?

Create more powerful applications.
What’s the benefit of Gigabit Ethernet?

Solve issues that 100 MBit can’t.
Industrial Gigabit Ethernet - the future of automation.